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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	3056.1US (96-803.1)
First Inventor or Application Identifier	Larry D. Kinsman
Title	VARIED-THICKNESS HEAT SINK FOR INTEGRATED CIRCUIT (IC) PACKAGES AND METHOD OF FABRICATING IC PACKAGES
Express Mail Label No.	EL500246104US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents
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1. [X] * Fee Transmittal Form *(e.g., PTO/SB/17)*
(Submit an original, and a duplicate for fee processing)
2. [X] Specification [Total Pages 24]
(preferred arrangement set forth below)
- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings *(if filed)*
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3 [X] Drawing(s) *(35 U.S.C 113)* [Total Sheets 2]

4 Oath or Declaration [Total Pages 2]
a [ ] Newly executed (original or copy)
b [X] Copy from a prior application (37 C F.R. § 1.63(d))
(for continuation/divisional with Box 17 completed)
[Note Box 5 below]
i [ ] DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

5. [X] Incorporation By Reference *(useable if Box 4b is checked)*
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. [ ] Microfiche Computer Program *(Appendix)*

7. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
a. [ ] Computer Readable Copy
b. [ ] Paper Copy (identical to computer copy)
c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet & document(s))
9. [ ] 37 C.F.R.§3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [X] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [ ] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
14. [ ] * Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application, Status still proper and desired
15. [ ] Certified Copy of Priority Document(s)
(if foreign priority is claimed)
16. [ ] Other. .....

** A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon.*

17. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in a preliminary amendment:*

[ ] Continuation [X] Divisional [ ] Continuation-in-part (CIP) of prior application No: 08 / 887,381

Prior application information: Examiner D. Graybill Group / Art Unit: 2814

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APPLICATION FOR LETTERS PATENT

for

VARIED-THICKNESS HEAT SINK FOR INTEGRATED CIRCUIT (IC) PACKAGES AND METHOD OF FABRICATING IC PACKAGES

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VARIED-THICKNESS HEAT SINK FOR INTEGRATED CIRCUIT (IC) PACKAGES AND METHOD OF FABRICATING IC PACKAGES

BACKGROUND OF THE INVENTION

Cross Reference to Related Applications: This application is a divisional of application Serial No. 08/887,381, filed July 2, 1997, pending. This application is related to a co-pending application entitled "LEAD FRAME ASSEMBLIES WITH VOLTAGE REFERENCE PLANE AND IC PACKAGES INCLUDING SAME," filed July 2, 1997, having Serial No. 08/888,336, now U.S. Patent 5,955,777, issued September 21, 1999, and commonly assigned with the present application.

Field of the Invention: The present invention relates in general to devices and methods for reducing lead inductance in integrated circuit (IC) packages and, more specifically, to heat sinks for reducing lead inductance in such packages, minimizing volume of heat sink material, enhancing retention of the heat sink in molded packages, and improving moldability of the package encapsulant.

State of the Art: Integrated circuit (IC) packages typically contain small, generally rectangular integrated circuits referred to as IC "dice" or "chips." These IC dice come in an almost infinite variety of forms, including, for example, Dynamic Random Access Memory (DRAM) dice, Static Random Access Memory (SRAM) dice, Synchronous DRAM (SDRAM) dice, Sequential Graphics Random Access Memory (SGRAM) dice, flash Electrically Erasable Programmable Read-Only Memory (EEPROM) dice, and processor dice.

Packaged IC dice communicate with circuitry external to their packages through lead frames embedded in the packages. These lead frames generally include an assembly of leads that extend into the packages to connect to bond pads on the IC dice through thin wire bonds or other connecting means and extend from the packages to terminate in pins or other terminals that connect to the external circuitry. Exemplary conventional lead frames include paddle-type wire-bond lead frames, which include a central die support and leads which extend to the perimeter of IC dice and connect to the dice through thin

wire bonds, Leads-Over-Chip (LOC) lead frames, having leads which extend over an IC die to attach to and support the die while being electrically connected to the die through wire bonds or other connecting means, and Leads-Under-Chip (LUC) lead frames, having leads which extend under an IC die to attach to and support the die from below while being connected to the die typically through wire bonds.

As with all conductors, the leads in lead frames have an inductance associated with them that increases as the frequency of signals passing through the leads increases. This lead inductance is the result of two interactions: the interaction among magnetic fields created by signal currents flowing to and from an IC die through the leads (known as "mutual" inductance); and the interaction between the magnetic fields created by the signal currents flowing to and from the IC die through the leads and magnetic fields created by oppositely directed currents flowing to and from ground (known as "self" inductance).

While lead inductance in IC packages has not traditionally been troublesome because traditionally slow signal frequencies have made the inductance relatively insignificant, the ever-increasing signal frequencies of state of the art electronic systems have made lead inductance in IC packages significant. For example, overall performance of IC dice attached to leads in IC packages is slower than desirable because the inductance associated with the leads slows changes in signal current through the leads, causing signals to take longer to propagate through the leads. Also, digital signals propagating along the leads are dispersing (i.e., "spreading out") because the so-called "Fourier" components of various frequencies that make up the digital signals propagate through the inductance associated with the leads at different speeds, causing the components, and hence the digital signals themselves, to disperse along the leads. While mild dispersion merely widens the digital signals without detrimental effect, severe dispersion can make the digital signals unrecognizable upon receipt. In addition, so-called "reflection" signals propagating along the leads as a result of impedance mismatches between the leads and IC dice or the leads and external circuitry caused, in part, by the inductance associated with the leads can distort normal signals propagating

along the leads at the same time as the reflection signals. Further, magnetic fields created by signal currents propagating through the inductance associated with the leads can induce currents in nearby leads, causing so-called "crosstalk" noise on the nearby leads. While these various effects can be troublesome in any electronic system, the modern trend toward 3.3 volt systems and away from 5.0 volt systems only serves to make these effects more noticeable and significant.

Prior IC packages have been configured in an attempt to reduce various effects of lead inductance as described above. For example, U.S. Patent No. 5,214,845, assigned to the assignee of the present invention, employs a flexible, laminated sandwich assembly of an outer ground plane and an outer power plane dielectrically isolated from a series of conductive traces running therebetween. The traces and planes are connected to corresponding bond pads on an IC die at one end, and to leads on the other, as by thermocompression bonding (in the case of a TAB embodiment), or by wire bonds. Such an arrangement obviously doubles the number of required I/O connections by requiring two connections for each lead, and thus necessitates additional assembly time and increases the possibility of a faulty connection. Further, the flexible sandwich assembly constitutes an additional element of the package, increasing material cost.

Another approach to reducing the inductance effects described above is disclosed in U.S. Patent No. 5,559,306, in which metal plates are employed above and below leads extending to the exterior of plastic and ceramic packages to effect reduction of self and mutual inductance. However, such configurations as disclosed appear to require relatively complex fabrication techniques to locate and fix the plates relative to the die and lead fingers or other conductors for subsequent transfer molding of a filled-polymer package thereabout, while the ceramic package embodiment is not cost-effective for high-volume, commercial packaging.

Accordingly, the inventors have recognized the need for a low-cost, reduced-inductance IC package configuration adaptable to current packaging designs and employing conventional and readily-available materials, equipment and fabrication techniques.

SUMMARY OF THE INVENTION

An inventive integrated circuit (IC) package includes a package body, such as an extruded plastic or ceramic package body, having an IC die positioned therein. The IC die may be, for example, a Dynamic Random Access Memory (DRAM) die, a Static Random Access Memory (SRAM) die, a Synchronous DRAM (SDRAM) die, a Sequential Graphics Random Access Memory (SGRAM) die, a flash Electrically Erasable Programmable Read-Only Memory (EEPROM) die, or a processor die.

A lead frame, such as a conventional peripheral lead, Leads-Over-Chip (LOC), or Leads-Under-Chip (LUC) lead frame, includes a plurality of leads with portions enclosed within the package body that connect to the IC die. A heat sink is positioned at least partially within the package body so a surface of a first portion of the heat sink faces the lead frame in close proximity to a substantial part, such as at least 80 percent, of the enclosed portion of each of the leads of the lead frame to thereby substantially reduce an inductance associated with each of the leads. The heat sink is preferably grounded so it acts as a ground plane for the leads, but it may also be electrically isolated, connected to a signal voltage, or connected to a reference voltage other than ground. A die-attach area on the surface of the first portion of the heat sink provides a support for the IC die, and a second portion of the heat sink is connected to the first portion substantially opposite the die-attach area and projects away from the first portion and the IC die to dissipate heat from the IC die.

The inventors have thus provided a low-cost, reduced-inductance IC package configuration adaptable to current packaging designs and employing conventional and readily-available materials, equipment and fabrication techniques.

Another embodiment of the present invention is directed toward the heat sink of the previously summarized embodiment. Still another embodiment is directed to an electronic system including input, output, processor, and memory devices, and one of the devices includes the previously summarized IC package embodiment.

A further embodiment of the present invention comprises a method of making an IC package that includes providing a lead frame comprising a plurality of leads having

portions for enclosure within the IC package. The enclosable portions of the leads of the lead frame are connected to an IC die, and an electrically conductive heat sink is positioned so a surface of a first portion of the heat sink faces the lead frame in close proximity to a substantial part of the enclosable portion of each of the leads of the lead frame to substantially reduce an inductance associated with each of the leads, so a die-attach area on the surface of the first portion may be attached to the IC die, and so a second portion of the heat sink connected to the first portion and substantially opposite the die-attach area projects away from the first portion and the IC die to dissipate heat from the IC die. The IC die is attached to the die-attach area on the surface of the first portion of the heat sink, and the enclosable portions of the leads of the lead frame, the IC die, and the heat sink are enclosed in the IC package.

A still further embodiment comprises a method of reducing an inductance associated with leads of a lead frame in an IC package. The leads have portions enclosed within the IC package and connected to an IC die. The method includes positioning an electrically conductive heat sink within the IC package so a surface of the heat sink faces the lead frame in close proximity to at least about 80 percent of the enclosed portion of the lead frame.

An additional embodiment comprises a lead frame assembly that includes a lead frame and a heat sink positioned with a surface in a substantially mutually parallel and co-extensive relationship with, and in close but electrically insulated proximity to, the lead frame.

A still additional embodiment comprises a method for assembling an IC package, such as a Leads Over Chip (LOC) or Leads Under Chip (LUC) package, that includes an IC die. The method includes providing a lead frame that includes a plurality of leads having portions for enclosure within the IC package, and providing an electrically conductive heat sink enclosable at least partially within the IC package with a surface of a first portion of the heat sink facing the lead frame in close proximity to a substantial part of the enclosable portion of each of the leads of the lead frame, with a die-attach area on the surface of the first portion attachable to the IC die, and with a second portion of the

heat sink projecting away from the first portion under the die-attach area. The lead frame is bonded to the heat sink, and the IC die is bonded to the die-attach area on the surface of the first portion of the heat sink. Also, the IC die is electrically connected to the leads of the lead frame, such as through wire bonds, and the heat sink is electrically connected to the lead frame.

A further embodiment comprises an IC package including a package body. An IC die is positioned within the package body along with portions of the leads of a lead frame that connect to the IC die. An electrically conductive heat sink is positioned at least partially within the package body with a vertically extending columnar portion surrounded by a horizontally extending skirt portion, and the skirt portion has a lead frame attachment surface proximate a die-attach surface substantially vertically aligned with the columnar portion. The lead frame attachment surface is attached to the lead frame and the die-attach surface is attached to the IC die.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

FIG. 1A is a cross-sectional side view of an integrated circuit (IC) package employing a heat sink to reduce lead inductance in the leads of a wire-bond lead frame in accordance with the present invention;

FIG. 1B is a cross-sectional side view of an IC package employing a heat sink to reduce lead inductance in the leads of a Leads-Over-Chip (LOC) lead frame in accordance with another embodiment of the present invention;

FIG. 1C is a cross-sectional side view of an IC package employing a heat sink to reduce lead inductance in the leads of a Leads-Under-Chip (LUC) lead frame in accordance with still another embodiment of the present invention; and

FIG. 2 is a block diagram of an electronic system including the IC package shown in FIG. 1C.

DETAILED DESCRIPTION OF THE INVENTION

As shown in a cross-sectional side view in FIG. 1A, an integrated circuit (IC) package 10 in accordance with the present invention includes a package body 12 formed of encapsulating material having an IC die 14 therein. It will be understood by those having skill in the field of this invention that any package body of encapsulating material will work for purposes of the invention, including, for example, transfer-molded plastic package bodies and preformed ceramic package bodies. It will also be understood that the present invention will work in combination with any IC die, including, for example, a Dynamic Random Access Memory (DRAM) IC die, a Static Random Access Memory (SRAM) IC die, a Synchronous DRAM (SDRAM) IC die, a Sequential Graphics Random Access Memory (SGRAM) IC die, a flash Electrically Erasable Programmable Read-Only Memory (EEPROM) IC die, a processor IC die, or any other suitable IC die. It will further be understood that the IC package 10 may comprise any IC package, including, for example, a Small Outline J-lead (SOJ) package, a Thin Small Outline Package (TSOP), a Vertical Surface Mount Package (VSMP), a Quad Flat Pack (QFP) or a Thin QFP (TQFP).

Bond pads (not shown) on the IC die 14 are connected to leads 16 of a conventional paddle-type wire-bond lead frame 18 through wire bonds 20 so signals may pass between the IC die 14 and circuitry (not shown) external to the IC package 10 connected to the leads 16. Although the present embodiment will be described with respect to a wire-bonded, peripheral-lead finger lead frame, it will be understood that the present invention is applicable to any lead frame, including, for example, Leads-Over-Chip (LOC) and Leads-Under-Chip (LUC) lead frames, as will be described in more detail below with respect to FIGS. 1B and 1C. It will also be understood that the present invention is not limited to wire-bonded connections between leads of a lead frame and an IC die. Rather, the present invention includes within its scope all forms of connection between the leads of a lead frame and an IC die, including, for example, conventional Tape-Automated Bonding (TAB) connections, thermocompression bonding connections, and conductive adhesive connections.

The IC die 14 is attached by its backside through a heat-conductive material 22, such as a eutectic solder or an epoxy adhesive, to a die-attach area in a recess 24 in a surface of a first portion 26 of an electrically conductive heat sink 28 so heat from the IC die 14 may be transferred to the heat sink 28. A second portion 30 of the heat sink 28 projects away from the first portion 26 and the IC die 14 so heat transferred from the IC die 14 will more readily dissipate to the ambient environment outside the IC package 10.

By projecting away from the first portion 26 of the heat sink 28 in this manner, the second portion 30 of the heat sink 28 also "locks" the heat sink 28 firmly in place within the transfer molded filled encapsulant of package body 12. Locking holes 17 may be included in the heat sink 28 to receive the transfer molded encapsulant of the package body 12 and thereby further "lock" the heat sink 28 in place within the package body 12.

A conventional heat sink, like the one shown in U.S. Patent No. 5,379,187, typically has difficulty "locking" in place within the transfer molded encapsulant of an IC package body because it generally comprises a single rectangular portion situated below an IC die which disrupts the even flow of encapsulant during manufacturing, causing the encapsulant to only loosely adhere to the heat sink. Such loose adherence between the encapsulant and a conventional heat sink in an IC package creates potential moisture paths between the package and its environment, and also makes the IC package more susceptible to cracking caused by moisture internal to the package.

In contrast, the heat sink 28 of the present invention includes the first portion 26 about which encapsulant may flow in a more even manner than with such conventional heat sinks. The first portion 26 also presents more surface area to which the encapsulant may adhere than the described conventional heat sinks. This increased adhesion or "locking" between the encapsulant and the heat sink 28 creates fewer potential moisture paths between the package and its environment during manufacturing, and thereby makes the IC package 10 less susceptible to cracking caused by moisture internal to the package 10. These improvements are reflected in better performance by the heat sink 28 of the present invention in comparison to the described conventional heat sinks in the well-known preconditioned reflow test (PRT), commonly known as the "popcorn" test,

which tests moisture intrusion in IC packages. The improvements are also reflected in better performance by the heat sink 28 of the present invention in the well known thermal cycling test, which tests IC packages for cracking mechanisms.

It will be understood that although the heat sink of the present embodiment is shown as having first and second portions integral with one another, the first and second portions of the heat sink, or the heat sink itself, may, instead, comprise a plurality of attached or interlocked parts, as will be described in more detail below with respect to FIGS. 1B and 1C. It will also be understood that although the second portion 30 of the heat sink 28 is shown as being generally rectangular, it can take any form that projects away from the first portion 26 and the IC die 14. It will further be understood that the second portion 30 of the heat sink 28 may extend beyond the exterior of the package body 12 of the IC package 10, as will be described below with respect to FIG. 1C.

The first portion 26 of the heat sink 28 extends beneath a substantial part of enclosed portions 32 of the leads 16 of the lead frame 18 in close proximity to the leads 16 but separated therefrom by an adhesive insulative layer 38, such as an adhesive tape or screen printed adhesive on the lead frame 18 or the heat sink 28. By extending in such close proximity to the leads 16, the first portion 26 of the heat sink 28 magnetically couples to the leads 16 and reduces the mutual and self inductance associated with the leads 16 as described above. A first portion 26 that extends beneath a "substantial part" of the enclosed portions 32 of the leads 16 includes, but is not limited to, those first portions that extend beneath substantially all of the enclosed portions of the leads 16, that extend substantially to sides 33 of the IC package 10 as shown in FIG. 1A, and that, for example, extend beneath at least about eighty percent (80%) of the area of the enclosed portions of the lead frame 18.

Those of skill in the field of this invention will recognize that the distance of the heat sink 28 from the leads 16, as well as the width of the heat sink 28, may be respectively decreased and increased to increase the effect of the heat sink 28 in reducing the inductance associated with the leads 16. Those of skill will also recognize that the heat sink 28 may be electrically isolated, or, preferably, may be connected to ground,

another reference voltage, or a signal voltage through a wire bond 34 to the IC die 14 or through welds 36 between the leads 16 and the heat sink 28. Of course, it will also be understood that the heat sink 28 may be connected to a grounded backside surface of the IC die 14, and hence to ground, through an electrically conductive solder or die-attach epoxy (not shown) between the heat sink 28 and the IC die 14, and that the heat sink 28 may be connected to one or more of the leads 16, and hence to ground or a signal voltage, through an electrically conductive adhesive (not shown) between the leads 16 and the heat sink 28, as will be described below with respect to FIG. 1B.

Test results have shown that in one IC package in which the heat sink of the present invention is electrically isolated, lead inductance is reduced from that of a conventional, electrically isolated heat sink by about 18 percent (from about 4.95 nanohenries (nH) to about 4.05 nH). Such results have also shown that in another IC package in which the heat sink of the present invention is connected to a signal voltage, lead inductance is reduced from that of a conventional heat sink connected to a signal voltage by about 25 percent (from about 4.60 nH to about 3.47 nH). Finally, test results have shown that in yet another IC package in which the heat sink of the present invention is grounded, lead inductance is reduced from that of a conventional, grounded heat sink by about 50 percent (from about 3.98 nH to about 1.96 nH).

As shown in a cross-sectional side view in FIG. 1B, an IC package 40 in accordance with another embodiment of the present invention includes a package body 42 encapsulating an IC die 44. Bond pads (not shown) on the IC die 44 are connected to leads 46 of an LOC lead frame 48 through wire bonds 50 so signals may pass between the IC die 44 and circuitry (not shown) external to the IC package 40 connected to the leads 46. Although the present embodiment will be described with respect to an LOC lead frame, it will be understood that the present invention is applicable to any lead frame, including, for example, LUC lead frames, as will be described in more detail below with respect to FIG. 1C, and wire-bond lead frames, as was described above with respect to FIG. 1A.

The IC die 44 is attached through a heat-conductive and electrically conductive material 52, such as a solder or an epoxy adhesive, to a die-attach area in a recess 54 in a surface of a first portion 56 of an electrically conductive heat sink 58 so heat from the IC die 44 may be transferred to the heat sink 58. A second portion 60 of the heat sink 58 projects away from the first portion 56 and the IC die 44 so heat transferred from the IC die 44 will more readily dissipate to the ambient environment outside the IC package 40. By projecting away from the first portion 56 of the heat sink 58 in this manner, the second portion 60 of the heat sink 58 also "locks" the heat sink 58 firmly in place within the transfer molded IC package 40 in a manner undisclosed by prior heat sinks. It will be understood that although the heat sink of the present embodiment is shown as having first and second portions each comprising a plurality of attached or interlocked parts, the first and second portions of the heat sink may, instead, be integral with one another, as described above with respect to FIG. 1A. It will also be understood that although the second portion 60 of the heat sink 58 is shown as being generally rectangular, it can take any form that projects away from the first portion 56 and the IC die 44. It will further be understood that the second portion 60 of the heat sink 58 may extend outside the IC package 40, as will be described below with respect to FIG. 1C.

The first portion 56 of the heat sink 58 extends beneath a substantial part of enclosed portions 62 of the leads 46 of the lead frame 48 in close proximity to the leads 46 but separated therefrom by an insulative layer 67. By extending in such close proximity to the leads 46, the first portion 56 of the heat sink 58 magnetically couples to the leads 46 and thereby reduces the mutual and self inductance associated with the leads 46 as described above. A first portion 56 that extends beneath a "substantial part" of the enclosed portions 62 of the leads 46 includes, but is not limited to, those first portions that extend beneath substantially all of the enclosed portions of the leads 46, that extend substantially to sides 63 of the IC package 40 as shown in FIG. 1B, and that extend beneath at least about eighty percent (80%) of the area of the enclosed portions of the lead frame 48.

Those of skill in the field of this invention will recognize that the distance of the heat sink 58 from the leads 46, as well as the width of the heat sink 58, may be respectively decreased and increased to increase the effect of the heat sink 58 in reducing the inductance associated with the leads 46. Those of skill will also recognize that the heat sink 58 may be electrically isolated, or, preferably, may be connected to a grounded backside surface of the IC die 44, and hence to ground, through the electrically conductive material 52, or connected to a signal voltage or ground through a conductive adhesive 66 between the leads 46 and the heat sink 58.

As shown in a cross-sectional side view in FIG. 1C, an IC package 70 in accordance with still another embodiment of the present invention includes a package body 72 encapsulating an IC die 74. Bond pads (not shown) on the IC die 74 are connected to leads 76 of an LUC lead frame 78 through wire bonds 80 so signals may pass between the IC die 74 and circuitry (not shown) external to the IC package 70 connected to the leads 76.

The IC die 74 is attached through a heat-conductive material 82, such as a solder or an epoxy adhesive, to a die-attach area on the leads 76, and the leads 76 are in turn attached to a surface of a first portion 86 of an electrically conductive heat sink 88 through a heat-conductive layer 83 so heat from the IC die 74 may be transferred to the heat sink 88. A second portion 90 of the heat sink 88 projects away from the first portion 86 and the IC die 74 and outside the IC package 70 so heat transferred from the IC die 74 will more readily dissipate to the ambient environment outside the IC package 70. By projecting away from the first portion 86 of the heat sink 88 in this manner, the second portion 90 of the heat sink 88 also "locks" the heat sink 88 firmly in place within the IC package 70 in a manner undisclosed by prior heat sinks. It will be understood that although the heat sink of the present embodiment is shown as comprising a plurality of attached or interlocked parts, the heat sink may, instead, be an integral whole, as described above with respect to FIG. 1A. It will also be understood that although the second portion 90 of the heat sink 88 is shown as being generally

rectangular, it can take any form that projects away from the first portion 86 and the IC die 74.

The heat sink 88 may be attached to a surface of a portion of a printed circuit board (PCB) 96, and may be grounded or connected to a signal or supply voltage through the attached portion of the PCB 96.

The first portion 86 of the heat sink 88 extends beneath a substantial part of enclosed portions 92 of the leads 76 of the lead frame 78 in close proximity to the leads 76 but separated therefrom by the heat conductive layer 83. By extending in such close proximity to the leads 76, the first portion 86 of the heat sink 88 magnetically couples to the leads 76 and thereby reduces the mutual and self inductance associated with the leads 76 as described above. A first portion 86 that extends beneath a "substantial part" of the enclosed portions 92 of the leads 76 includes, but is not limited to, those first portions that extend beneath substantially all of the enclosed portions 92 of the leads 76, that extend substantially to sides 93 of the IC package 70 as shown in FIG. 1C, and that extend beneath at least eighty percent (80%) of the enclosed portions 92 of the lead frame 78.

Those of skill in the field of this invention will recognize that the distance of the heat sink 88 from the leads 76, as well as the width of the heat sink 88, may be respectively decreased and increased to increase the effect of the heat sink 88 in reducing the inductance associated with the leads 76. Those of skill will also recognize that the heat sink 88 may be electrically isolated, or, preferably, may be connected to a signal voltage or ground as previously described.

As shown in a block diagram in FIG. 2, an electronic system 100 includes an input device 102, an output device 104, a processor device 106, and a memory device 108. The memory device 108 includes an IC package 70 as described above with respect to FIG. 1C, although it will, of course, be understood that the electronic system 100 may include any one of the IC packages of FIGS. 1A, 1B, and 1C in any one of the input, output, processor, and memory devices 102, 104, 106, and 108.

Although the present invention has been described with reference to particular embodiments, the invention is not limited to these described embodiments. Rather, the invention is limited only by the appended claims, which include within their scope all equivalent devices or methods that operate according to the principles of the invention as described.

CLAIMS

What is claimed is:

1. An integrated circuit (IC) package comprising:

a package body;

an IC die positioned within the package body;

a lead frame including a plurality of leads having portions enclosed within the package body that connect to the IC die; and

an electrically conductive heat sink positioned at least partially within the package body with a surface of a first portion of the heat sink facing the lead frame in close proximity to a substantial part of the enclosed portion of each of the leads of the lead frame and with a die-attach area on the surface of the first portion attached to the IC die, a second portion of the heat sink projecting away from the first portion under the die-attach area and the IC die.

2 The IC package of claim 1, wherein the package body is selected from a group comprising a transfer molded plastic package body and a preformed ceramic package body.

3. The IC package of claim 1, wherein the IC die is selected from a group comprising a Dynamic Random Access Memory (DRAM) IC die, a Static Random Access Memory (SRAM) IC die, a Synchronous DRAM (SDRAM) IC die, a Sequential Graphics Random Access Memory (SGRAM) IC die, a flash Electrically Erasable Programmable Read-Only Memory (EEPROM) IC die, and a processor IC die.

4. The IC package of claim 1, wherein the lead frame is selected from a group comprising a peripheral-lead finger lead frame, a Leads Over Chip (LOC) lead frame, and a Leads Under Chip (LUC) lead frame.

5. The IC package of claim 1, wherein the heat sink is coupled to one of a signal voltage and a reference voltage so the heat sink operates respectively as a signal plane and a ground plane for the leads of the lead frame.

6. The IC package of claim 5, wherein the heat sink is coupled to the reference voltage through one of a wirebond, a conductive adhesive, and a welded connection.

7. The IC package of claim 1, wherein the heat sink is electrically isolated from the lead frame.

8. The IC package of claim 1, wherein the heat sink is positioned only partially within the package body.

9. The IC package of claim 1, wherein the heat sink is coupled to a printed circuit board outside the package body and is thereby coupled to one of a signal voltage and a reference voltage so the heat sink operates respectively as a signal plane and a ground plane for the leads of the lead frame.

10. The IC package of claim 8, wherein the second portion of the heat sink projects substantially to one of a top and a bottom of the package body.

11. The IC package of claim 1, wherein the heat sink is positioned within the package body with the surface of its first portion in close proximity to substantially all of the enclosed portion of each of the leads of the lead frame.

12. The IC package of claim 1, wherein the heat sink is positioned within the package body with its first portion extending substantially to at least one side of the package body.

13. The IC package of claim 1, wherein the heat sink is positioned within the package body with the surface of its first portion in close proximity to at least eighty percent of an area of the enclosed portion of the lead frame.

14. The IC package of claim 1, wherein the first and second portions of the heat sink are integral with one another.

15. The IC package of claim 1, wherein the first and second portions of the heat sink comprise separate parts.

16. The IC package of claim 1, wherein the heat sink comprises a plurality of parts, each forming a portion of both the first and second portions of the heat sink.

17. The IC package of claim 1, wherein the surface of the first portion of the heat sink includes a recess in which the die-attach area is located.

18. The IC package of claim 1, wherein the heat sink has locking holes therein for locking the heat sink in the IC package.

19. The IC package of claim 1, further comprising an adhesive attaching the lead frame to the heat sink.

20. The IC package of claim 1, wherein the IC package comprises one of a Vertical Surface Mount Package (VSMP), a Small Outline J-lead (SOJ) package, a Thin Small Outline Package (TSOP), a Quad Flat Pack (QFP), and a Thin QFP (TQFP).

21. A heat sink for an integrated circuit (IC) package having a lead frame including a plurality of leads having portions enclosed within the IC package that connect to an IC die, the heat sink comprising:

a first portion having a surface constructed to face the lead frame in close proximity to a substantial part of the enclosed portion of each of the leads of the lead frame, a die-attach area on the surface of the first portion being attachable to the IC die; and

a second portion substantially opposite the die-attach area for projecting away from the first portion under the die-attach area and the IC die.

22. An electronic system comprising an input device, an output device, a memory device, and a processor device coupled to the input, output, and memory devices, at least one of the input, output, memory, and processor devices including an integrated circuit (IC) package comprising:

a package body;

an IC die positioned within the package body;

a lead frame including a plurality of leads having portions enclosed within the package body that connect to the IC die; and

an electrically conductive heat sink positioned at least partially within the package body with a surface of a first portion of the heat sink facing the lead frame in close proximity to a substantial part of the enclosed portion of each of the leads of the lead frame and having a die-attach area on the surface of the first portion attached to the IC die, a second portion of the heat sink being opposite the die-attach area and projecting away from the first portion and the IC die.

23. A lead frame assembly comprising:

a lead frame; and

a heat sink positioned with a surface in a substantially mutually parallel and co-extensive relationship with, and in close but electrically insulated proximity to, the lead frame.

24. An integrated circuit (IC) package comprising:

a package body;

an IC die positioned within the package body;

a lead frame including a plurality of leads having portions enclosed within the package body that connect to the IC die; and

an electrically conductive heat sink positioned at least partially within the package body with a vertically extending columnar portion surrounded by a horizontally extending skirt portion having a lead frame attachment surface proximate a die-attach surface substantially vertically aligned with the columnar portion, the lead frame attachment surface being attached to the lead frame and extending in close proximity to a substantial part of the enclosed portions of the leads of the lead frame, the die-attach surface being attached to the IC die.

25 An integrated circuit (IC) package comprising:

an IC die,

a lead frame including a plurality of leads having portions that are connected to the IC die; and

an electrically conductive heat sink positioned having a surface of a first portion of the heat sink facing the lead frame in close proximity to a substantial part of the enclosed portion of each of the leads of the lead frame and with a die-attach area on the surface of the first portion attached to the IC die, a second portion of the heat sink projecting away from the first portion under the die-attach area and the IC die.

26. The IC package of claim 25, further comprising:

a package body.

27. The IC package of claim 26, wherein the package body is selected from a group comprising a transfer molded plastic package body and a preformed ceramic package body.

28. The IC package of claim 25, wherein the IC die is selected from a group comprising a Dynamic Random Access Memory (DRAM) IC die, a Static Random Access Memory (SRAM) IC die, a Synchronous DRAM (SDRAM) IC die, a Sequential Graphics Random Access Memory (SGRAM) IC die, a flash Electrically Erasable Programmable Read-Only Memory (EEPROM) IC die, and a processor IC die.

29. The IC package of claim 25, wherein the lead frame is selected from a group comprising a peripheral-lead finger lead frame, a Leads Over Chip (LOC) lead frame, and a Leads Under Chip (LUC) lead frame.

30. The IC package of claim 25, wherein the heat sink is coupled to one of a signal voltage and a reference voltage so the heat sink operates respectively as a signal plane and a ground plane for the leads of the lead frame.

31. The IC package of claim 30, wherein the heat sink is coupled to the reference voltage through one of a wirebond, a conductive adhesive, and a welded connection.

32. The IC package of claim 25, wherein the heat sink is electrically isolated from the lead frame.

33. The IC package of claim 26, wherein the heat sink is positioned only partially within the package body.

34. The IC package of claim 26, wherein the heat sink is coupled to a printed circuit board outside the package body and is thereby coupled to one of a signal voltage and a reference voltage so the heat sink operates respectively as a signal plane and a ground plane for the leads of the lead frame.

35. The IC package of claim 34, wherein the second portion of the heat sink projects substantially to one of a top and a bottom of the package body.

36. The IC package of claim 26, wherein the heat sink is positioned within the package body with the surface of its first portion in close proximity to substantially all of the enclosed portion of each of the leads of the lead frame.

37. The IC package of claim 26, wherein the heat sink is positioned within the package body with its first portion extending substantially to at least one side of the package body

38. The IC package of claim 26, wherein the heat sink is positioned within the package body with the surface of its first portion in close proximity to at least eighty percent of an area of the lead frame.

39. The IC package of claim 25, wherein the first and second portions of the heat sink are integral with one another.

40. The IC package of claim 25, wherein the first and second portions of the heat sink comprise separate parts.

41. The IC package of claim 25, wherein the heat sink comprises a plurality of parts, each forming a portion of both the first and second portions of the heat sink.

42. The IC package of claim 25, wherein the surface of the first portion of the heat sink includes a recess in which the die-attach area is located.

43. The IC package of claim 25, wherein the heat sink has locking holes therein for locking the heat sink in the IC package.

44. The IC package of claim 25, further comprising an adhesive attaching the lead frame to the heat sink.

45. The IC package of claim 25, wherein the IC package comprises one of a Vertical Surface Mount Package (VSMP), a Small Outline J-lead (SOJ) package, a Thin Small Outline Package (TSOP), a Quad Flat Pack (QFP), and a Thin QFP (TQFP).

ABSTRACT OF THE DISCLOSURE

An inventive integrated circuit (IC) package includes a package body, such as a transfer molded plastic or preformed ceramic package body, having an IC die positioned therein. A lead frame, such as a peripheral lead, Leads-Over-Chip (LOC), or Leads-Under-Chip (LUC) lead frame, includes a plurality of leads with portions enclosed within the package body that electrically connect to the IC die. A heat sink is positioned at least partially within the package body so a surface of a first portion of the heat sink faces the lead frame in close proximity to a substantial part, such as at least eighty percent, of the area of the enclosed portion of the lead frame to thereby substantially reduce an inductance associated with each of the leads. The heat sink is preferably grounded so it acts as a ground plane for the leads, but it may also be electrically isolated from the lead frame, or connected to a signal voltage. A die-attach area on the surface of the first portion of the heat sink is attached to the IC die, and a second portion of the heat sink is connected to the first portion substantially opposite the die-attach area and projects away from the first portion and the IC die to dissipate heat from the IC die.

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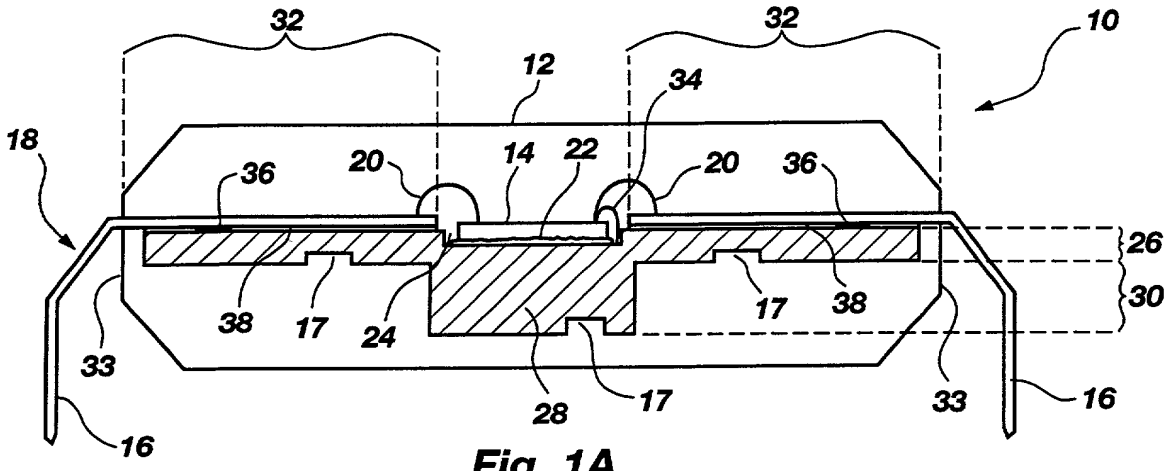

Fig. 1A

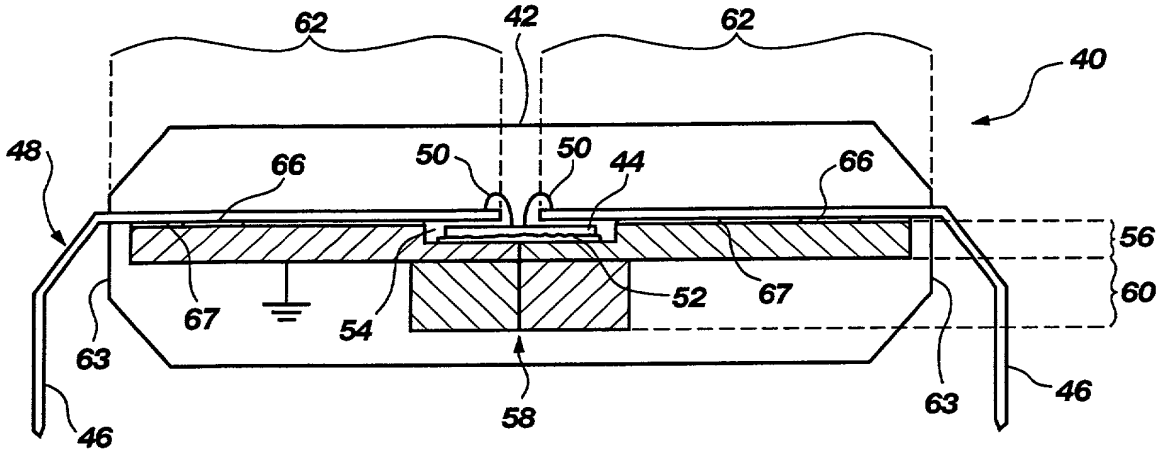

Fig. 1B

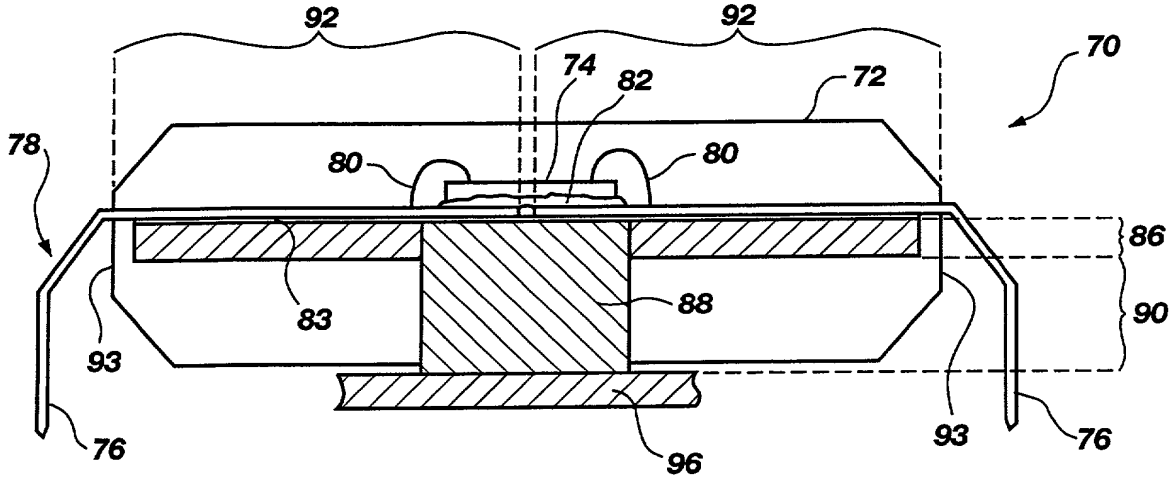

Fig. 1C

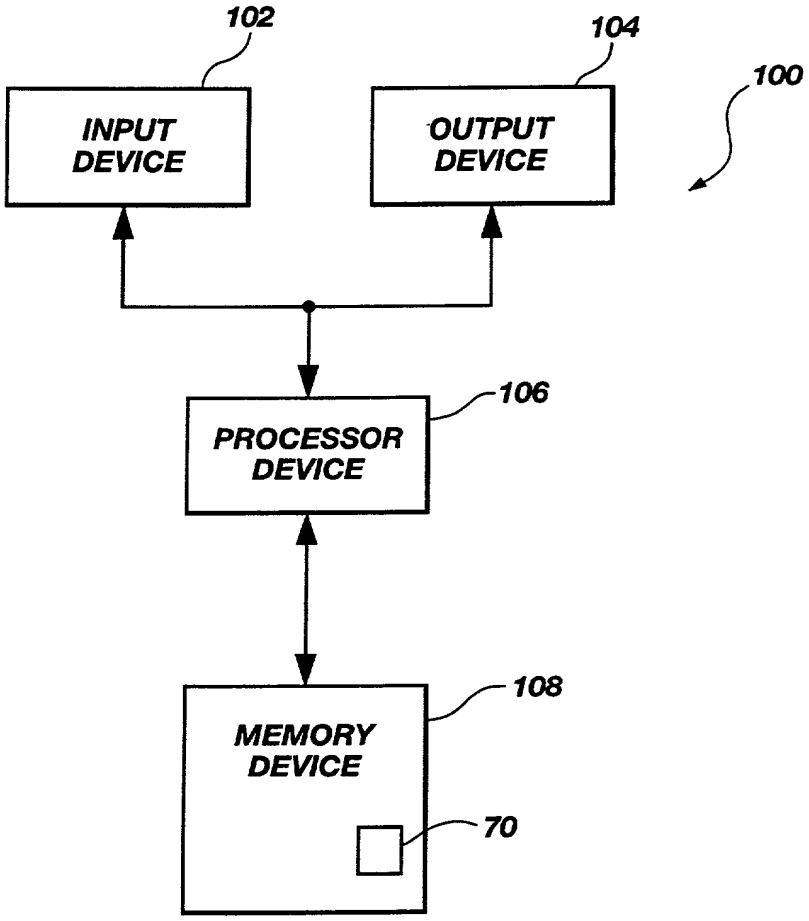
102
104
100
INPUT DEVICE
OUTPUT DEVICE
106
PROCESSOR DEVICE
108
MEMORY DEVICE
70

Fig. 2

DECLARATION FOR PATENT APPLICATION (WITH POWER OF ATTORNEY)

As an inventor named below or on any attached continuation page, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name.

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled VARIED-THICKNESS HEAT SINK FOR INTEGRATED CIRCUIT (IC) PACKAGES AND METHOD OF FABRICATING IC PACKAGES, the specification of which (check one):

- ☒ is attached hereto.
- ☐ was filed on _____ as United States application serial no. _____ and was amended on _____.
- ☐ was filed on _____ as PCT international application no. _____ and was amended under PCT Article 19 on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to the patentability of the subject matter claimed in this application, as "materiality" is defined in Title 37, Code of Federal Regulations § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 (a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate or § 365(a) of any PCT international application(s) designating at least one country other than the United States of America listed below and on any attached continuation page and have also identified below and on any attached continuation page any foreign application for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America having a filing date before that of the application(s) on which priority is claimed.

Prior foreign/PCT application(s):

(number)	(country)	(day/month/year filed)	Priority Claimed Yes	No

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or § 365(c) of PCT international application(s) designating the United States of America listed below and on any attached continuation page and, insofar as the subject matter of each of the claims of this application is not disclosed in any such prior application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations § 1.56 which became available between the filing date of such prior application and the national or PCT international filing date of this application:

(application serial no.)	(filing date)	(status - pending, patented or abandoned)

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

(provisional application no.)	(filing date)

I hereby appoint the following Registered Practitioners to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of first joint inventor: Larry D. Kinsman
Inventor's signature Larry D. Kinsman Date 6/2/97
Residence: Boise, ID 83706
Citizenship: USA
Post Office Address: HC33 Box 2461, Boise, ID 83706-9736

DECLARATION FOR PATENT APPLICATI
(continuation page)

Invention title: VARIED-THICKNESS HEAT SINK FOR INTEGRATED CIRCUIT (IC) PACKAGES AND METHOD OF FABRICATING IC PACKAGES

Inventor name(s) appearing on first declaration page: Larry D. Kinsman

☒ Additional original, first and joint inventor(s):

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